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VERIFICATION OF A TRANSLATION

I, Susan ANTHONY BA, ACIS,

Director of RWS Group Ltd, of Europa House, Marsham Way, Gerrards Cross, Buckinghamshire, England declare:

That the translator responsible for the attached translation is knowledgeable in the French language in which the below identified international application was filed, and that, to the best of RWS Group Ltd knowledge and belief, the English translation of the international application No. PCT/FR02/04433 is a true and complete translation of the above identified international application as filed.

I hereby declare that all the statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the patent application issued thereon.

Date: June 15, 2004

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METHOD AND DEVICE FOR CONVERTING A QUANTIZED DIGITAL VALUE

The present invention relates to the field of fixed-point digital signal processing. Applications may be found for it in any fixed-point digital system, and particularly in the digitally modulated synthesizers used in the radio transmitters and the radio transceivers of a digital radiocommunication system.

For carrying out operations on binary numbers, a floating-point digital system comprises software resources such as a correctly programmed DSP (Digital Signal Processor). A fixed-point system, however, only comprises sequential logic circuits such as digital adders, digital multipliers, shift registers or the like.

The binary numbers which are processed by a fixed-point digital system encode quantized values corresponding to a real value X (for example the variable value of the radio signal received by a radio receiver, or the constant value of the frequency of a radio channel). These quantized numbers are represented by integers between zero and 2^n-1 - where n is the number of bits used for encoding the information - if the value X is always positive, or between $-(2^n-1)$ and 2^n-1 if the value X is signed (that is, if it can be negative). By convention, Xq denotes the quantized value which is obtained from the real value X by a quantizing operation. For linear quantizing, the correspondence between the real value X (so-called real information) and the quantized value Xq (so-called quantized information) is given by the relation:

$$Xq = \text{round}(X \times Cq) \qquad (1)$$

where Cq is a real number referred to as the quantization coefficient.

The quantization of the system is determined by the number Cq in relation with the number n. The quantization coefficient Cq is such that:

$$\begin{cases} \text{round}(|X(t)|xCq) \leq 2^{n-1} - 1, \forall t, \text{if the inf ormation X is signed} \\ \text{round}(X(t)xCq) \leq 2^{n} - 1, \forall t, \text{otherwise} \end{cases} \quad (2)$$

where |x| denotes the absolute value operator of the real variable x.

The act of quantizing the information X creates an error, referred to as the quantization error and denoted by e, such that:

$$e = X - \frac{Xq}{Cq} = X - \frac{\text{round}(X \times Cq)}{Cq} \quad (3)$$

The error e is of course variable, inasmuch as it depends on the value X. According to the properties of the rounding function, the error e is always such that $|e| \leq \frac{1}{2 \times Cq}$. The maximum value of the quantization error, denoted by e_{max}, is therefore given by:

$$e_{max} = \frac{1}{2 \times Cq} \quad (4)$$

The inverse of the quantization coefficient Cq is the resolution of the digital system, that is to say the smallest variation of the real information which is distinguishable in the quantized information. Put another way, $\frac{1}{Cq}$ is such that if $X = \frac{1}{Cq} + X'$ then $Xq = 1 + Xq'$.

Optimization of the dynamic range of the system generally leads to the quantization being defined by choosing Cq such that:

$$\begin{cases} Cq = \frac{\max(|X(t)|)}{2^{n-1} - 1}, \forall t, \text{if the information X is signed} \\ Cq = \frac{\max(X(t))}{2^{n} - 1}, \forall t, \text{otherwise} \end{cases} \quad (5)$$

Certain systems dictate the quantization of the digital data, for example in order to be compatible with analog signals after digital-analog conversion of a quantized signal. In this case, there is a quantization error majored in modulus by $e_{max} = \frac{1}{2 \times Cq}$, where Cq is the corresponding quantization coefficient.

However, it may arise that this resolution is insufficient for representing some or all of the digital signals of the system.

On the other hand, certain digital systems use constant digital values. In a radio transmitter or receiver, for example, such a digital constant may represent the central frequency of a radio channel. In this case, the situation may be encountered in which a quantization error affecting the digital constant (this error being systematic inasmuch as it does not vary) exceeds the maximum tolerable error for digital representation of this constant. If the system does not dictate the quantization of the digital data, then the systematic quantization error affecting a specific digital constant K may be reduced, albeit this may mean that the dynamic range of the system is not optimized, by choosing the quantization coefficient Cq such that $K-\frac{\text{round}(K \times Cq)}{Cq} \leq e_d \leq e_{max}$, where e_d is the maximum tolerable error for digital representation of the constant K. This is not always possible in a system which dictates the quantization of the digital data, such as a digitally modulated frequency synthesizer, for example.

This is why it is a first object of the invention to reduce the quantization errors of a digital signal and/or to digitally correct a systematic quantization error of a digital value (in particular a constant value) without any constraint governing the quantization, that is to say without any constraint governing n and Cq.

It is moreover possible for digital data obtained from two subsystems, having respective quantizations determined by distinct quantization coefficients, to be used in a digital system only if one of the two quantization coefficients is an integer multiple of the other.

Specifically, if data obtained from a first subsystem, having a quantization determined by a first

coefficient Cq1, are intended to be used in the same digital system with digital data obtained from a second subsystem, having a quantization determined by a second coefficient Cq2 different to Cq1, then Cq1 and/or Cq2 must be chosen such that Cq2 = r×Cq1 or Cq1 = r×Cq2, where r is an integer.

The data can then be rendered uniform by multiplying the data of the first subsystem or of the second subsystem, as applicable, by r. This, however, is only possible if at least one of the subsystems does not dictate the quantization of the digital data.

This is why it is a second object of the invention to allow a plurality of digital systems to be connected together, while insuring compatibility of the data but without any constraints governing their respective quantizations.

A first aspect of the invention thus provides a method for converting a digital input value quantized according to a first quantization coefficient and encoded over and most n1 bits, into a digital output value quantized according to a second quantization coefficient and encoded over at most n2 bits, where n1 and n2 are nonzero integers.

The method comprises the steps consisting in:

a) multiplying the digital input value by an integer B encoded over at most β bits, where β is a nonzero integer, in order to generate a first intermediate digital value encoded over at most $n1+\beta$ bits; and

b) fixed-point dividing said first intermediate digital value by the number 2^{α}, where α is an integer less than or equal to $n1+\beta$, in order to generate said digital output value.

According the invention, the number $\frac{B}{2^{\alpha}}$ is substantially equal to the ratio of said second quantization coefficient to said first quantization coefficient. Step b) is furthermore carried out by means of a sigma-delta modulator (Σ-Δ modulator). This

is preferably a 1^{st} order Σ-Δ modulator, which is the simplest to use.

It will be noted that digital/digital conversion is involved, that is to say both the digital output value and the digital input value are quantized digital values. What changes is the quantization of this digital value. In particular, the Σ-Δ modulator is a digital/digital modulator.

A second aspect of the invention also provides a device for converting a digital input value quantized according to a first quantization coefficient and encoded over at most n1 bits, into a digital output value quantized according to a second quantization coefficient and encoded over at most n2 bits, where n1 and n2 are nonzero integers.

The device comprises multiplier means for multiplying the digital input value by an integer B encoded over at most β bits, where β is a nonzero integer. These multiplier means generate a first intermediate digital value encoded over at most n1+β bits. The device furthermore comprises divider means for fixed-point dividing said first intermediate digital value by the number 2α, where α is an integer less than or equal to n1+β. These divider means generate said digital output value.

According the invention, the number $\frac{B}{2^{\alpha}}$ is substantially equal to the ratio of said second quantization coefficient to said first quantization coefficient. Said divider means furthermore comprise a sigma-delta (Σ-Δ) modulator.

As is known, a Σ-Δ modulator is a circuit synchronous with the sampling frequency of the input signal. It performs quantization "noise shaping" at the high frequencies. A signal with a reduced quantization noise at the useful frequencies is recovered at the output of the Σ-Δ modulator. On average, that is to say

at a low frequency compared with the sampling frequency, the gain of the device is equal to $\frac{B}{2^{\alpha}}$.

A digital output value which corresponds, with good precision, to the digital input value multiplied by the ratio of said second quantization coefficient to the first quantization coefficient is therefore obtained at the output of the Σ-Δ modulator.

The principle of the invention is based on the following concept. In what follows, Sq1 will denote the digital input value (quantized information) and Cq1 will denote the first quantization coefficient. Likewise, Sq2 will denote the digital output value (quantized information) and Cq2 will denote the second quantization coefficient. Lastly, S will denote the real value (unquantized information) corresponding to Sq1 and Sq2. The relations below are then written:

$$Sq2 = \text{round}(S \cdot Cq2) \tag{6}$$

$$\text{whence } Sq2 \cong \text{round}(S \cdot Cq1) \cdot \frac{Cq2}{Cq1} \tag{7}$$

$$\text{whence } Sq2 \cong Sq1 \cdot \frac{Cq2}{Cq1} \tag{8}$$

$$\text{that is to say } Sq2 \cong Sq1 \cdot \frac{B}{2^{\alpha}} \tag{9}$$

$$\text{with } \frac{Cq2}{Cq1} \cong \frac{B}{2^{\alpha}} \tag{10}$$

It can be seen that the effect of the invention is to implement relation (9) by using relation (10). It therefore makes it possible to convert the digital value Sq1 into a digital value Sq2, which are information quantized according to different respective quantization coefficients Cq1 and Cq2 and which both correspond to the same real information S, without any restrictive assumption being made about the relation between one of these quantization coefficients and the other.

The invention thus makes it possible to reduce the quantization error affecting a variable or constant real value. Specifically, it is sufficient to choose the first quantization coefficient Cq1 so as to

minimize the quantization error affecting the digital value Sq1, and to convert this value by delivering it as a digital input value to a device according to the invention, in order to obtain a digital output value Sq2 quantized according to a second quantization coefficient Cq2, which will be chosen as being that of the quantization of the subsystem needing to use the digital input value. The quantization error affecting the digital value Sq2 can thus be reduced without any constraints governing the quantization of the subsystem.

This is shown by the following calculation of the quantization error e affecting the real value S, in the case when the device according to the invention is used.

The expression for e is given by:

$$e = S - \frac{\left(Sq1 \cdot \frac{B}{2^{\alpha}}\right)}{Cq2} \qquad (11)$$

But Sq1 = round(S.Cq1).

Whence $|Sq1| \leq |S.Cq1| + \frac{1}{2}$ and $-Sq1 \leq -S.Cq1 + \frac{1}{2}$

From this it follows:

$$e \leq S - \frac{\left(S.Cq1 \cdot \frac{B}{2^{\alpha}}\right)}{Cq2} + \frac{1}{2} \cdot \frac{\left(\frac{B}{2^{\alpha}}\right)}{Cq2}$$

$$\text{i.e. } |e| \leq |S| \cdot \left|1 - \frac{Cq1}{Cq2} \cdot \frac{B}{2^{\alpha}}\right| + \frac{1}{2} \cdot \frac{\left(\frac{B}{2^{\alpha}}\right)}{Cq2} = |S| \cdot \left|1 - \frac{Cq1}{Cq2} \cdot \frac{B}{2^{\alpha}}\right| + \frac{1}{2 \cdot Cq1} \cdot \left(\frac{Cq1}{Cq2} \cdot \frac{B}{2^{\alpha}}\right)$$

The choice of B and α gives $\frac{Cq1}{Cq2} \cdot \frac{B}{2^{\alpha}} = 1 + \varepsilon$, where ε denotes a negligible quantity compared with unity (ε = o(1)). It then follows:

$$|e| \leq |S| \cdot |\varepsilon| + \frac{1}{2 \cdot Cq1} \cdot (1 + \varepsilon) \cong |S| \cdot |\varepsilon| + \frac{1}{2 \cdot Cq1} \qquad (12)$$

The quantization error of the quantized value Sq2 obtained by the method according to the invention is therefore at most equal to the sum, on the one hand, of the maximum quantization error of the value Sq1

quantized according to the quantization coefficient Cq1 and, on the other hand, an image of the real value S which will in general be negligible. With a quantization according to the quantization coefficient Cq2, there would have been an error majored by $\frac{1}{2 \cdot Cq2}$.

In order to reduce the quantization error affecting the value of Sq2 in the subsystem that uses this value, the value of Cq1 will advantageously be chosen such that Cq1 is greater than Cq2 (Cq1 > Cq2).

In the particular case when the digital value in question is an integer, the first digital input value Sq1 is equal to the real value S (Sq1 = S) and the first quantization coefficient Cq1 is equal to unity (Cq1 = 1). The quantization error affecting Sq1 is then zero, and the quantization error affecting Sq2 is then minimal. In this case, relation (12) is written:

$$e = S \times \varepsilon \qquad (13)$$

The invention furthermore makes it possible for a digital value Sq1 of a first subsystem, having a first specific quantization, to be adapted to a second specific quantization which is associated with a second subsystem that needs to use this digital value, without any constraints governing the respective quantizations of these two subsystems. Specifically, it is sufficient to deliver this digital value Sq1 as a digital input value to a device according to the invention, in which said first quantization coefficient Cq1 is chosen to be equal to that of said first specific quantization, and in which said second quantization coefficient Cq2 is chosen to be equal to that of said second specific quantization.

A third aspect of the invention provides a digitally modulated frequency synthesizer, comprising a phase-locked loop comprising a variable-ratio frequency divider in the return path. The division ratio of said divider is controlled by a digital value obtained in particular from a real value corresponding to the

central frequency of a radio channel. The synthesizer furthermore comprises a conversion device as defined, for reducing the quantization error affecting said real value.

Other characteristics and advantages of the invention will moreover become apparent on reading the description which follows. This description is purely illustrative and should be read with reference to the appended drawings, in which:

- Figure 1 is a block diagram of a device according to the invention;
- Figure 2 is a flow chart of the steps in a method according to the invention;
- Figure 3 is a block diagram of a first embodiment of the device in Figure 1;
- Figure 4 is a block diagram of a second embodiment of the device in Figure 1;
- Figure 5 is a diagram illustrating the application of a mask to a specific digital value;
- Figure 6 is a block diagram of a third embodiment of the device in Figure 1; and
- Figure 7 is a block diagram of a digitally modulated synthesizer incorporating a device according to the invention.

Figure 1 represents the block diagram of a device according to the invention.

The device comprises an input 1 for receiving a digital input value Sq1, which is a quantized value of a variable or constant real value. The value Sq1 is quantized according to a first quantization coefficient Cq1 and encoded over at most n1 bits, where n1 is a nonzero integer. The device also comprises an output 2 for delivering a digital output value Sq2. The value Sq2 is quantized according to a second quantization coefficient Cq2 and encoded over at most n2 bits, where n2 is a nonzero integer.

The device also comprises means, such as a digital multiplier 10, for multiplying the digital input value Sq1 by an integer B encoded over at most β

bits, where β is a nonzero integer. The means 10 generate a first intermediate digital value C encoded over at most $n1+\beta$ bits.

The device further comprises divider means for fixed-point dividing said first intermediate digital value C by the number 2^{α}, where α is an integer less than or equal to $n1+\beta$. These divider means generate the digital output value Sq2.

According to the invention, these divider means comprise a sigma-delta modulator 20, which receives the intermediate value C as input and delivers the digital output value Sq2 as output. The Σ-Δ modulator is a digital/digital modulator, which receives as input a digital value encoded over $n1+\beta$ bits and delivers as output a digital value encoded over $n1+\beta+1-\alpha$ bits. It is preferably a 1^{st} order Σ-Δ modulator, which is the simplest to use. Embodiments with a higher-order Σ-Δ modulator may nevertheless be envisaged.

According to the invention, the number $\frac{B}{2^{\alpha}}$ is furthermore substantially equal to the ratio $\frac{Cq2}{Cq1}$ of the second quantization coefficient Cq2 to the first quantization coefficient Cq1.

As mentioned in the introduction, such a device converts the digital value Sq1, quantized according to the quantization coefficient Cq1, into the digital value Sq2, quantized according to the quantization coefficient Cq2.

Figure 2 is a flow chart illustrating the steps in a method according to the invention. The method is carried out by a device as described above with reference to Figure 1.

In a step 100, the digital input value Sq1 is received.

In a step 200, the value Sq1 is multiplied by the number B in order to generate the first intermediate digital value C.

In a step 300, the first intermediate digital value C is fixed-point divided by the number 2^{α} in order to generate the digital output value Sq2. According to the invention, step 300 is carried out by means of a sigma-delta modulator. The number $\frac{B}{2^{\alpha}}$ is furthermore substantially equal to the ratio $\frac{Cq2}{Cq1}$.

The diagram in Figure 3 illustrates a first embodiment of a device according to the invention, which is suitable for carrying out a first variant of the method.

In this first embodiment, the sigma-delta modulator 20 comprises means 21 such as a digital adder, which receive as input the first intermediate digital value C as a first operand, on the one hand, and a digital error value E as a second operand, on the other hand. The latter is encoded over at most α bits. The means 21 deliver as output a second intermediate digital value D encoded over at most $n1+\beta+1$ bits.

The device further comprises selection means 23, such as a digital discriminator, for selecting the n2 most significant bits of the second intermediate digital value D as the digital output value Sq2, and for selecting the α least significant bits of said second intermediate digital value D as the digital error value E. It follows that n2 is equal to $n1+\beta+1-\alpha$. The means 23 receive the value D as input and deliver the value Sq2 as well as the value E as output.

A digital discriminator is a circuit which separates the k high-significance bits and the j low-significance bits of a given digital input value in order to generate two digital output values, encoded respectively over k bits and over j bits and each having as its value the value corresponding respectively to said k high-significance bits and to the j low-significance bits. Here, the discriminator 23 separates the $n1+\beta+1-\alpha$ most significant bits of the second intermediate digital value D, on the one hand,

and the α least significant bits of the value D, on the other hand.

The diagram in Figure 4 illustrates a second embodiment of a device according to the invention, which is suitable for carrying out a second variant of the method.

In this second embodiment, the selection means 23 of the device comprise an operator 24 for shifting to the right by α bits. Such an operator is formed, for example, with the aid of a properly controlled shift register. This operator 24 receives as input the $n1+\beta+1$ bits of the second intermediate digital value D. It delivers as output the $n1+\beta+1-\alpha$ most significant bits of the second intermediate digital value D as a digital output value Sq2.

The selection means 23 furthermore comprise means 25 for applying a mask to the second intermediate digital value D.

Such a mask is represented in Figure 5 with the reference M. It is a digital value stored in an appropriate register and having at most $n1+\beta+1$ bits, the $n1+\beta+1-\alpha$ most significant bits of which are equal to the logical value 0 and the α least significant bits of which are equal to the logical value 1. When it is combined with the second intermediate digital value D in an operation of the logical AND type, it makes it possible to select the α least significant bits of said second intermediate digital value D.

Stated otherwise, the means 25 receive as input the $n1+\beta+1$ bits of the second intermediate digital value D. They deliver as output the $n1+\beta+1-\alpha$ most significant bits of the second intermediate digital value D as the digital error value E.

The diagram in Figure 6 illustrates a third embodiment of a device according to the invention, which is suitable for carrying out a third variant of the method.

In this third embodiment, the selection means 23 of the device still comprise an operator 24 for

shifting to the right by α bits, which has the same function as the operator 24 of the device in Figure 4.

The selection means 23 further comprise an operator 26 for shifting to the left by α bits, which receives as input the $n1+\beta+1-\alpha$ bits of the digital output value Sq2 and delivers as output a third intermediate digital value F, encoded over at most $n1+\beta+1$ bits. The operator 26 is, for example, a properly controlled shift register. They furthermore comprise an operator 27 for taking the difference between the intermediate digital values F and C. The operator 27 is, for example, a digital subtracter. It receives the third intermediate digital value F as a first operand, and the first intermediate digital value C as a second operand. It delivers as output the digital error value E.

In each of the three embodiments described above with reference to Figures 3, 4 and 6, the device preferably comprises an operator 22 that applies a unitary delay to the digital error value E for synchronization reasons. Stated otherwise, the error signal E is delivered to the input of the adder means 21 through a unitary delay operator 22.

Figure 6 shows the diagram of a digitally modulated frequency synthesizer, more commonly referred to by the term DMS, which incorporates a device according to the invention.

Such a circuit can be used for generating a frequency- or phase-modulated radiofrequency signal (in the UHF band lying between 400 and 600 MHz). Applications may be found for it in the radio transmitters or transceivers of a radiocommunication system, particularly in the base stations and/or the mobile terminals of such a system.

A DMS has a structure which is derived from the structure of a fractional N frequency synthesizer, and makes it possible to generate a frequency- or phase-modulated periodic signal.

The DMS includes a phase-locked loop or "PLL", comprising a phrase/frequency comparator 11 or "PFC", a loop filter 12 such as an integrator, and a voltage controlled oscillator 13 or "VCO" in series in a forward channel, and as well as a frequency divider 14 in a return channel. The VCO delivers as output a signal S_{out} which is the output signal of the DMS, the instantaneous frequency of which is f_{out}. The PFC receives at a first input a reference signal S_{ref} having a reference frequency f_{ref}, and at a second input a signal S_{div} delivered by the frequency divider 14 on the basis of the signal S_{out}.

For conventional fractional N synthesis, the frequency divider 14 is a variable-ratio divider making it possible to produce the signal S_{div} by dividing the frequency f_{out} of the signal S_{out} by a division ratio, which alternately has the value of an integer N for a part of the time T1 and the integer N+1 for the rest of the time T2. In this way, the frequency f_{out} of the output signal S_{out} is given as a function of the frequency f_{ref} of the reference signal S_{ref} by:

$$f_{out} = \left(N + \frac{T1}{T1+T2} \right) \times f_{ref} \qquad (14)$$

In a digitally modulated synthesizer, the frequency divider 14 includes an input for controlling the division ratio. This ratio is fixed by the value stored in a specific accumulator. In order to prevent spurious lines, due to periodicity of the division ratio changes from N to N+1 and back again, from occurring in the spectrum of the output signal S_{out}, however, a DMS known in the prior art furthermore includes a modulator 15 of the digital/digital Σ-Δ modulator type.

The modulator 15 includes an input which receives a digital frequency- or phase-modulation value S_{mod} encoded over k bits, and an output which delivers a digital value S'_{mod}, corresponding to the processed value S_{mod} and encoded over j bits. The output of the modulator 15 is connected to a first input of a digital

adder 16, the second input of which receives a digital value N_o that defines the bottom of the frequency band addressed by the synthesizer. The output of the adder 16 delivers a digital value S_c. It is connected to the control input of the divider 14 in order to deliver the value S_c to it.

The DMS also comprises a second digital adder 17, a first input of which receives a digital value S_{info} and a second input of which receives a digital value S_{ch2}. The output of the adder 17 delivers the aforementioned digital frequency- or phase-modulation value S_{mod}. The digital value S_{info} contains the modulation information (modulating signal), that is to say the useful information to be transmitted. The digital value S_{ch2} corresponds to the central frequency of the radio channel (after the aforementioned value N_o has been added).

The digital values S_{info}, S_{ch2}, S_{mod} and S'_{mod} and N_o are values that are quantized according to a quantization coefficient Cq2 of the digital system constituted by the DMS.

According to the invention, the value S_{ch2} is delivered by a converter device 18 as described above with reference to Figures 2 to 6, on the basis of a digital value S_{chq1} stored in an appropriate register. The quantized values S_{ch1} and S_{ch2} correspond to a real value, namely the central frequency of the channel, denoted below by F_{ch}. The real value F_{ch} is constant, because the central frequency of the channel is constant. If the device 18 was not there, the real value F_{ch} would be directly quantized according to the quantization coefficient Cq2 of the digital system constituted by the DMS. However, the DMS presented here incorporates a device 18 according to the invention in order to reduce the quantization error affecting the quantized digital value corresponding to the real value F_{ch} (which is a systematic error since this value is constant). Stated otherwise, the DMS comprises a device 18 for converting the digital value S_{ch1} into a digital

value S_{ch2}, which is quantized according to the quantization coefficient Cq2 of the digital system constituted by the DMS.

To apply that which has been described above, a choice is therefore made to implement a converter device 18 of the type described above, for which Cq1 is equal to unity (Cq1 = 1, because the real value F_{ch} is integer) and for which Cq2 is the quantization coefficient of the quantization of the DMS.

A numerical example for illustrating the advantages offered by the invention in this application will be given below. In this example:

- F_{ref} = 9.6 MHz (megahertz);
- k = 22;
- j = 4;
- F_{ch} = 400017.5 kHz (kilohertz);
- N_o = round(395 MHz/F_{ref});
- e_d = 4 Hz (hertz).

The frequency resolution of such a DMS is given by $\frac{F_{ref}}{2^{k-j}}$, where k is the number of bits at the input of the sigma-delta modulator 15, and where j is the number of bits at the output of this modulator. The frequency resolution of the DMS, that is to say $\frac{1}{Cq2}$, is therefore:

$$\frac{1}{Cq2} = \frac{F_{ref}}{2^{k-j}} = \frac{9.6 \cdot 10^6}{2^{18}} \approx 36.62 \text{ Hz}$$

The value F_{min}, corresponding to the bottom of the frequency band addressed by the DMS, is determined by the digital value N_o according to the relation $F_{min} = N_o \times F_{ref}$. Here, therefore, $F_{min} = 41 \times 9.6 \cdot 10^6 = 393.6$ MHz.

Let us first consider what the situation would be without the device 18 according to the invention, that is to say if Sch1 = Sch2. We would have:

Fch2 = round[$(F_{ch}-F_{min}).Cq2$] = 175241

The systematic quantization error affecting the central frequency of the radio channel would therefore be:

$$e = F_{ch} - \left(\frac{Fch2}{Cq2} + F_{min}\right)$$

i.e.:

$$e = 400017.5 \cdot 10^3 - \left(\frac{175241}{Cq2} + 393.6 \cdot 10^6\right) = -17.08 \text{ Hz}$$

This value exceeds (in absolute value) the acceptable error e_d.

Let us now consider what happens with the conversion device 18 according to the invention. Since the signal intended to be represented is integer, we have Cq1 = 1.

The following approximation is chosen: $Cq2 \approx \frac{B}{2^\alpha} = \frac{229065}{2^{23}}$. In other words, a choice is made to implement a device according to the invention with B = 229065 and $\alpha = 23$.

The quantization error can be determined by using the relation (13) given in the introduction, which is valid in the case when the real digital value at the input of the device (here, the constant value $F_{ch}-F_{min}$) is an integer. It will be recalled that this relation is then written:

$$e = S.\varepsilon = S. \quad \frac{Cq1}{Cq2} \quad \frac{B}{2^\alpha} \quad 1 \quad \cong 2.17 \text{ Hz}$$

where S denotes the real digital value at the input of the device (here F_{ch}).

Whence it follows that $e \cong 2.17$ Hz. The goal of a quantization error less than 4 Hz affecting the value of the central frequency of the radio channel has therefore indeed been achieved, without having to modify the quantization of the system. Here, the invention makes it possible to reduce the systematic quantization error affecting the value of the central frequency of the radio channel from 17 Hz to 2 Hz.

A better result could be obtained by increasing the precision of the approximation for $\frac{Cq2}{Cq1}$, but at the cost of increasing the number β and the number α.